

IN THE SPECIFICATION:

Please amend paragraph number [0004] as follows:

[0004] There is typically a large mismatch in the coefficient of thermal expansion (CTE) between the material of the semiconductor die and that of the carrier substrate, such as a circuit board or interposer, bearing the conductive traces to which the external conductive elements of the die are bonded. Thus, significant lateral stresses between the semiconductor die and carrier substrate result from normal thermal cycling. Without a strong mechanical attachment of the semiconductor die to the substrate, the die might pop loose from the carrier substrate, or one or more of the external conductive elements might fracture or release from its corresponding conductive trace. In addition, the small spacing or pitch of the external conductive elements creates a significant potential for shorting between adjacent conductive elements or conductive elements and adjacent carrier substrate traces due to the presence of a dust particle or condensed moisture between the semiconductor die and the carrier substrate. Therefore, when a flip-chip type of electronic-device device, such as a semiconductor-die die, is conductively attached to a carrier substrate, underfilling the space between the device and substrate with an electrically insulative material is very desirable to enhance the mechanical bond between the die and the substrate and to mutually laterally dielectrically isolate adjacent electrical connections between the die and the carrier substrate.

Please amend paragraph number [0008] as follows:

[0008] As shown in FIG. 1, adequate removal of air, water vapor and condensed moisture from the interstitial volume or spaces 34, particularly the crevices 36 at connector interfaces with the active surface 22 and carrier substrate 10, is not consistently achieved. Voids or bubbles 26 of gas or condensed, liquid water may remain in the underfill structure 38 in the interstitial volume or spaces 34 and may conductively join external conductive elements 30, plurality of conductive pads 32 and conductive trace pads 14 to provide a short circuit. Moreover, the material of the underfill structure 38 does not adhere to all of the surfaces of

semiconductor die 20 and carrier substrate 10 in the interconnection area under the “footprint” of the die, thus lessening the mechanical bond strength therebetween. Furthermore, the so-called Fine Ball Grid Array (FBGA) now in use in the semiconductor industry, using very small-dimensioned balls and ball-pitch pitch, as well as typically a reduced spacing between adjacent semiconductor dice on a carrier substrate and the disposition of dice on both sides of a carrier substrate, limits the use of vacuum apparatus to enhance the effective underfill between dice and the carrier substrate. As a result, the manufacture of such electronic assemblies results in high cost and a relatively high reject and rework rate, which is obviously very costly.

Please amend paragraph number [0014] as follows:

[0014] However, to the inventor’s knowledge, stereolithography has yet to be applied to mass production of articles in volumes of thousands or millions millions, or employed to produce, augment augment, or enhance products including flip-chip semiconductor devices in large quantities, where minute component sizes are involved, and where extremely high resolution and a high degree of reproducibility of results is required. Furthermore, stereolithography methods have not been used to package, at the wafer level, large numbers of flip-chip dice of the same or differing configurations to provide underfilled or even packaged devices which that become environmentally sealed upon bonding to a carrier-substrate substrate, such as a printed circuit board (PCB). In such a method, the difficulties of precisely locating a number of pre-existing components for stereolithographic application of material thereto without the use of mechanical alignment techniques is required to assure precise, repeatable placement of encapsulant material.

Please amend paragraph number [0015] as follows:

[0015] The present invention comprises a method for underfilling semiconductor device assemblies including including, semiconductor dice (either pre-encapsulated or unencapsulated) which that are conductively connected to a carrier substrate. The invention further encompasses methods for both underfilling and encapsulating semiconductor devices

connected to a carrier substrate. In one embodiment of these methods, a dense packing of chip scale packages (CSP) having fine ball grid arrays (FBGA) of less than 1 mm ball pitch may be provided on a carrier substrate wherein the mechanical and electrical reliability of the apparatus is much enhanced by an improved underfill structure. The method provides an underfill structure ~~which~~ that is essentially free of voids, i.e., bubbles of air, water vapor, other vapors or gases or liquid ~~moisture~~ moisture, and which securely bonds to the semiconductor device and carrier substrate. Optionally, a complete package may be formed about a semiconductor device continuously with the underfill structure and in the same process. A very tightly packed array of semiconductor devices may be formed on a substrate and completely underfilled, and optionally encapsulated as well, using a stereolithographic process.

Please amend paragraph number [0016] as follows:

[0016] In one embodiment, the method of the invention comprises attaching the external conductive elements of one or more semiconductor dice to conductors on a carrier substrate to form a semiconductor device assembly and tilting the semiconductor device assembly so formed to an angle of about 10 to 90 degrees from the horizontal, followed by progressively immersing the tilted semiconductor device assembly in a reservoir of liquid, photopolymerizable resin of low viscosity to drive air, moisture, etc. from spaces between the semiconductor devices and the substrate, completely filling those spaces with liquid resin. Optionally, the semiconductor device assembly or the liquid resin may be vibrated during immersion to enhance removal of voids or bubbles from the interstices surrounding the external conductive elements comprising connections between the die or dice and the carrier substrate. For example, sonic or ultrasonic vibrations may be applied to the liquid resin, to the apparatus containing the ~~resin~~ resin, or to the semiconductor device assembly while the semiconductor device assembly is submerged. The semiconductor device assembly is then leveled to the horizontal while submerged within the volume of resin and raised vertically to a position wherein a substantially uniform, thin layer of liquid photopolymer resin overlies the carrier substrate face. A computer controlled STL laser beam is then traversed over the upper surface of the carrier

substrate and around the semiconductor dice mounted thereon to polymerize portions of the thin resin layer and form a semisolid or solid dam structure about each semiconductor die attached to the substrate face. As desired, the semiconductor device assembly is then lowered to provide a further thin layer of liquid photopolymer resin above the prior polymerized layer of the dam structure and a laser beam traversed again to polymerize the subsequently formed liquid layer atop the previously formed photopolymerized layer and to bond the new solid or semisolid layer to that previously formed, thus increasing the height of the dam structures. The layering steps may be repeated as many times as necessary or desired to reach the full height of the dam structure surrounding each semiconductor die and optionally bonded thereto to entrap a pool of unpolymerized liquid resin between each semiconductor die and the carrier substrate. If desired, additional layers may be formed to and over the back sides of the downwardly facing semiconductor dice to define encapsulating structures contiguous with the dam structures and overcovering the semiconductor dice. Preferably, but not necessarily, the dam structures, in combination with the semiconductor dice and the carrier substrate, sealingly contain the pools of unpolymerized resin between each die and the carrier substrate.

Please amend paragraph number [0018] as follows:

[0018] The method of the invention produces a substantially void-free dielectric underfill structure ~~which that~~ is substantially fully bonded to both the active surface of the semiconductor die (or its encapsulating layer if previously packaged) and to the carrier substrate face, as well as to the interposed external conductive connectors of the ball grid array (BGA). Thus, the semiconductor die-to-carrier substrate mechanical bond strength is greatly enhanced to avoid breakage or disconnection of external conductive ~~elements~~ elements, such as solder balls. Further, the opportunity for shorting between (and environmental deterioration of) external conductive elements, bond pads and substrate traces is substantially eliminated. If desired, the stereolithography process may be continued to completely encapsulate the entire semiconductor device assembly (but for any connections to any yet-higher level packaging) with an imperforate protective structure.

Please amend paragraph number [0019] as follows:

[0019] The use of stereolithography in the inventive method provides a very precisely configured dam structure of polymer-~~which that~~ is at least partially cured and ~~which~~ contains a reservoir of unpolymerized liquid-~~polymer~~ polymer, which is subsequently solidified in a separate thermal or other curing step.

Please amend paragraph number [0022] as follows:

[0022] Precise mechanical alignment of singulated semiconductor devices or larger semiconductor substrates having multiple device locations is not required to practice the method of the present invention, which includes the use of machine vision to locate devices and features or other components-~~thereon thereon~~ thereon, or associated-~~therewith therewith~~ therewith, or features on a larger substrate for alignment and material disposition purposes. The laser beam of the STL apparatus may be aimed using fiducial marks on the substrate-~~which that~~ are used to align the semiconductor devices before placement on the substrate, the shape of the-~~devices devices~~ devices, or any other fixed reference point-~~which that~~ provides device location.

Please amend paragraph number [0023] as follows:

[0023] In a preferred embodiment, dam formation and encapsulation for mounted electronic devices according to the invention use precisely focused electromagnetic radiation in the form of an ultraviolet (UV) wavelength laser under control of a computer and responsive to input from a machine vision-~~system system~~ system, such as a pattern recognition system to fix or cure a low-viscosity liquid material in the form of a photopolymer in situ.

Please amend paragraph number [0026] as follows:

[0026] FIG. 1 is a lateral cross-sectional view of a portion of a substrate and connected flip-chip configured semiconductor device-~~which that~~ has been underfilled in accordance with a method of the prior art;

Please amend paragraph number [0045] as follows:

[0045] In FIG. 3, exemplary semiconductor dice 20 are illustrated as having a flip-chip configuration, each bearing a ball grid array (BGA) of external conductive elements 30 30, such as, solder balls or conductive or conductor-filled epoxy on active surface 22, and having a backside 18 and lateral sides 24. The external conductive elements 30 are shown as being bonded to the plurality of conductive pads 32 on the active surface 22 and to conductive trace pads 14 on the carrier substrate face 12. The external conductive elements 30 may be bonded to the conductive trace pads 14 by heat-induced reflow in the case of solder or by curing in the case of epoxy, using any effective method such as is known in the art.

Please amend paragraph number [0046] as follows:

[0046] As depicted in FIGS. 3 and 4, a support structure or underfill structure 50 formed of polymerized ~~material~~ material essentially fills the interstitial volume or spaces 34 between each semiconductor die 20 and the carrier substrate 10, including the crevices 36 where the external conductive elements 30 meet the active surface 22 and the carrier substrate face 12. The underfill structure 50 is tightly adhered to the active surface 22 and the carrier substrate face 12 to mechanically attach the semiconductor die 20 to the carrier substrate 10. Contiguous with the underfill structure 50 is a structure or envelope 48 of protective ~~polymer~~ polymer, which is shown as covering the four lateral sides 24 and backside 18 of each semiconductor die 20. The underfill structure 50, together with the envelope 48 form a polymeric protective package ~~which~~ that seals and protects each semiconductor dice 20. Because of the unique method by which the underfill structure 50 is formed, there are essentially no bubbles of air or other gas, water vapor, or moisture within the underfill structure 50. Thus, any opportunity for mutual short-circuiting between external conductive elements 30, the plurality of conductive pads 32, and conductive trace pads 14 is virtually eliminated.

Please amend paragraph number [0047] as follows:

[0047] FIG. 5 shows a portion of semiconductor device assembly 40 to which the invention is applied and depicts various dimensions ~~which~~ that affect the manufacture of such apparatus. The carrier substrate 10 has a carrier substrate face 12 to which any number of semiconductor dice 20 may be attached. In this example, each flip-chip semiconductor die 20 has an active surface 22 bearing the plurality of conductive pads 32 to which solder ball external conductive elements 30 are mounted.

Please amend paragraph number [0049] as follows:

[0049] It is generally desirable to minimize the lateral spacing 39 between adjacent semiconductor dice 20 on a given carrier substrate so as to enhance operational speed of the semiconductor device assembly 40 and minimize use of substrate materials, as well as minimizing overall bulk of the semiconductor device assembly 40. Thus, the current trend is toward higher and higher densities of semiconductor dice 20 on a carrier substrate 10, to enhance miniaturization and reduce overall cost. The increased market share of laptop and notebook computers and the recent, significant reductions in size and weight ~~of~~ of the same also incentivizes the use of smaller semiconductor device assemblies. The lateral device spacing 39 may be different in different directions. As will be described below, the method of this invention facilitates the use of chip-scale packaged semiconductor dice 20 mounted at high density on a carrier substrate 10, reliably and fully underfilled and optionally fully encapsulated over the semiconductor dice backsides 18 and lateral sides 24.

Please amend paragraph number [0050] as follows:

[0050] The vertical or transverse device-to-substrate spacing 42 between the semiconductor die 20 and the carrier substrate 10 is determined by the size of the external conductive elements 30 (such as the diameter 44 of solder balls or the height of column or pillar-style conductive elements), type of external conductive elements 30 and other factors, such as bond pad and terminal height. In current practice, the device-to-substrate spacing 42 may be,

by way of example only, any value on the order of about 1 mil to about 28 mils (about 0.025 to about 0.66 mm) and will become smaller as the industry develops external conductive elements 30 of smaller size. Furthermore, advances in making complex semiconductor devices typically require an increase in the number of external connections even as device size is being reduced. The use of smaller external conductive elements 30 and a reduced element pitch 46 results in a much more dense packing of ~~devices~~ devices, such as semiconductor dice 20 on a carrier substrate 10, with a reduced lateral spacing 52 between adjacent external conductive elements 30. In the current state of the art, so-called ball grid arrays (BGA) may use external conductive elements 30, such as solder ball elements, having a pitch 46 of greater than about 1 mm. So-called fine ball grid arrays (FBGA) use an element pitch 46 of less than about 1 mm, and the resulting device-to-substrate spacing 42 is relatively small. It is evident that such dense, external conductive element lateral packing demands special care to purge and avoid the reentry of contaminants in the connector region, and the short device-to-substrate spacing 42 makes effective underfilling more difficult.

Please amend paragraph number [0056] as follows:

[0056] In the example provided herein, the semiconductor device assembly 40 is passed downwardly into the liquid photopolymer resin 60 in a direction 68A parallel to the carrier substrate face 12, or a direction 68B-~~which~~ that approaches the vertical, or a direction 68C-~~which~~ that is less than angle 64, or a direction 68D-~~which~~ that exceeds 90 degrees from the horizontal. The preferred direction of immersion is generally parallel with the carrier substrate face 12, plus or minus about 20 degrees.

Please amend paragraph number [0058] as follows:

[0058] FIG. 7 schematically illustrates a stereolithographic apparatus 100 for contaminant purging, underfilling and optionally encapsulating a plurality of flip-chip semiconductor dice 20 mounted on a carrier substrate 10. The apparatus 100 is shown in a purge mode, wherein semiconductor device assembly 40 is mounted on a support surface 122 of a

manipulatable support platform 120, tilted and immersed in a reservoir of liquid photopolymer resin 60. Platform 120 is supported by and manipulated in a vertical direction 82 and preferably in a horizontal direction 84 as well, by motion actuator 80 acting through arm 74. The motion actuator-80, as well as the generator 72, vibration element 76 or 78 are controlled by a program operating in computer (microprocessor) 102 and stored in memory 106.

Please amend paragraph number [0062] as follows:

[0062] Turning now to FIG. 8, various components and operation of an exemplary stereolithographic apparatus 100 are shown schematically to facilitate the reader's understanding of the technology employed in implementation of the present invention, although those of ordinary skill in the art will understand and appreciate that apparatus of other designs and manufacture may be employed in practicing the method of the present invention. The preferred, basic stereolithography apparatus 100 for implementation of the present invention as well as operation of such apparatus are described in great detail in United States patents assigned to 3D Systems, Inc. of Valencia, California, such patents including, without limitation, U.S.-~~Patents~~ Patent Nos. 4,575,330; 4,929,402; 4,996,010; 4,999,143; 5,015,424; 5,058,988; 5,059,021; 5,096,530; 5,104,592; 5,123,734; 5,130,064; 5,133,987; 5,141,680; 5,143,663; 5,164,128; 5,174,931; 5,174,943; 5,182,055; 5,182,056; 5,182,715; 5,184,307; 5,192,469; 5,192,559; 5,209,878; 5,234,636; 5,236,637; 5,238,639; 5,248,456; 5,256,340; 5,258,146; 5,267,013; 5,273,691; 5,321,622; 5,344,298; 5,345,391; 5,358,673; 5,447,822; 5,481,470; 5,495,328; 5,501,824; 5,554,336; 5,556,590; 5,569,349; 5,569,431; 5,571,471; 5,573,722; 5,609,812; 5,609,813; 5,610,824; 5,630,981; 5,637,169; 5,651,934; 5,667,820; 5,672,312; 5,676,904; 5,688,464; 5,693,144; 5,695,707; 5,711,911; 5,776,409; 5,779,967; 5,814,265; 5,840,239; 5,854,748; 5,855,718; and 5,855,836. The disclosure of each of the foregoing patents is hereby incorporated herein by this reference. As noted in more detail below, however, a significant modification is made to conventional stereolithographic apparatus, such as those offered by 3D Systems, Inc., in the context of initiation and control of the stereolithographic disposition and fixation of materials. Specifically, the apparatus of the present invention employs a so-called

“machine vision” system in combination with suitable programming of the computer controlling the stereolithographic process, to eliminate the need for accurate positioning or mechanical alignment of workpieces to which material is stereolithographically applied, and expands the use of conventional stereolithographic apparatus and methods to application of materials to large numbers of workpieces ~~which that~~ may differ in orientation, size, thickness, and surface topography. Additional detail regarding the use of machine vision on the context of stereolithography is disclosed in U.S. patent application Serial No. 09/259,142 filed February 26, 1999 and assigned to the assignee of the present invention, the disclosure of which patent application is hereby incorporated herein by this reference.

Please amend paragraph number [0063] as follows:

[0063] With reference again to FIGS. 7 and 8 and as noted above, a 3-D CAD drawing of a structure (such as a protective wall or dam and its component layers 90A, 90B, 90C, etc. see FIG. 17) to be fabricated in the form of a data file is placed in the memory 106 of a computer 102 controlling the operation of apparatus 100, if computer 102 is not a CAD computer in which the original object design is effected. In other words, an object design may be effected in a first computer, not shown, in an engineering or research facility and the data files transferred via wide or local area network, tape, disc, CD-ROM or otherwise as known in the art to computer 102 of apparatus 100 for object fabrication.

Please amend paragraph number [0068] as follows:

[0068] Data from the STL files resident in computer 102 and specifically in memory 106 is manipulated to build a structure ~~which that~~ in this invention comprises a dam structure 56 and/or encapsulation envelope 48 (see FIGS. 3 and 13) for each semiconductor die 20, one layer or slice 90A, 90B, 90C, etc. (see FIGS. 12 through 17) at a time. An effective scanning of each layer or slice included within the structures 56, 48 of all semiconductor dice 20 of the entire semiconductor device assembly 40 is preferably effected in one continuous operation.

Please amend paragraph number [0071] as follows:

[0071] In some instances a substrate support or supports 116 for nearly perfectly horizontally supporting the semiconductor device assembly 40 may also be programmed as a separate STL file, such supports 116 being fabricated before the overlying semiconductor device assembly 40 is placed thereon. The supports 116 facilitate fabrication of structure 56, 48 on semiconductor device assembly 40 with reference to a perfectly horizontal plane and removal of the structure from support surface 122 of platform 120. Where a “recoater” blade 118 (FIG. 8) is employed as described below, the interposition of substrate supports 116 precludes inadvertent contact of blade 118 with platform 120.

Please amend paragraph number [0072] as follows:

[0072] Before fabrication of a structure is initiated with apparatus 100, the primary STL file for the structure 56 and/or envelope 48 and the file for base substrate(s) 116 are merged. It should be recognized that, while reference has been made to a single structure or object, multiple objects may be concurrently fabricated at a level above support surface 122 of platform 120. For example, in this invention, a large number of flip-chip semiconductor dice 20 may be mounted on a carrier substrate-10_10, which is in turn mounted on support platform 120. The semiconductor dice 20 may have differing configurations (e.g., length, width and height) requiring differing STL file input. In such an instance, the STL files for the various differing structures 56 and/or envelope 48 for each semiconductor die 20 and supports 116 (if any) for semiconductor device assembly 40 on platform 120, may be merged.

Please amend paragraph number [0074] as follows:

[0074] Before initiation of a first layer 90A for a support 116 or structure 56 and/or envelope 48 is commenced, computer 102 automatically checks and, if necessary, adjusts by means known in the art as referenced above, the surface level 62 of liquid material 60 in reservoir 104 to maintain same at an appropriate focal length for laser beam 112. U.S.-Patent Patent No. 5,174,931, referenced above and previously incorporated herein by reference,

discloses one suitable level control system. Alternatively, the height of beam mirror 114 may be adjusted responsive to a detected surface level 62 to cause the focal point of laser beam 112 to be located precisely at the surface of liquid resin 60 at surface level 62 if surface level 62 is permitted to vary, although this approach is somewhat more complex.

Please amend paragraph number [0075] as follows:

[0075] With reference to FIGS. 8 and 9, the platform 120 is shown as being submerged in liquid material 60 in reservoir 104 to a depth above the carrier substrate face 12 equal to the thickness of one layer or slice 90 of a dam structure 56 to be fabricated, as in FIGS. 10-15. The liquid surface level 62 is adjusted as required to accommodate liquid resin 60 displaced by submergence of platform 120 and the semiconductor device assembly 40 thereon.

Please amend paragraph number [0076] as follows:

[0076] FIG. 10 depicts the in situ stereolithographic formation of a first structure layer 90A on carrier substrate face 12. Laser 108 is activated so that laser beam 112 will scan liquid resin 60 over portions of the liquid surface 62 to at least partially cure (e.g., at least partially polymerize) liquid resin 60 at selected locations to an at least semisolid state. Each scanned location defines the boundaries of an at least semisolid layer 90A (of dam structure 56, not shown, for example) example, which is further scanned to fill in the enclosed portions of the layer. The first layer 90A has a height 96A 96A, which is equivalent to the depth 92A (FIG. 9) of liquid layer 94A (FIG. 9) from which the layer 90A was formed.

Please amend paragraph number [0077] as follows:

[0077] Where the structure 56 and/or envelope 48 is to be formed from more than one polymerized layer 90 of resin 60, the process outlined above is repeated at a higher elevation. As shown in FIG. 11, platform 120 (FIG. 8) is lowered by a depth 92B of liquid layer 94B equal to the height 96B of a second layer 90B, and the laser beam 112 scanned again (FIG. 12) to define

and fill in the second layer 90B (FIG. 12), while simultaneously bonding the second layer to the first layer 90A.

Please amend paragraph number [0078] as follows:

[0078] Any number of layers 90 may be formed to attain the desired dam structure 56 which that joins the carrier substrate face 12 to all lateral sides 24 of the semiconductor die 20, depending on the device-to-substrate spacing 42, the layer thickness, the particular liquid resin 60 which is used, etc. Thus, the process may be further repeated to form additional layers 90 of the structure 56. Any structure formed by this method may constitute a single layer 90 or a plurality of layers.

Please amend paragraph number [0082] as follows:

[0082] The STL-formed structure 56 then undergoes postcuring, as the laser treated resin may be only partially polymerized and exhibit only a portion (typically 40% to 60%) of its fully cured strength. In addition, it is necessary to cure the unpolymerized liquid resin 60 trapped between the semiconductor die 20 and carrier substrate 10. Postcuring to completely harden the structure(s) 56 and/or envelope 48 may be effected in another apparatus which that will cure the unexposed resin 60. Typically, the postcure will be thermal in nature and will form a singular structure from the dam structure 56 and trapped, subsequently cured resin 60. The formed structure is securely adhered to the active surface 22 or device surface 23, to portions of lateral sides 24 or 88, and to the carrier substrate face 12, as shown in FIG. 14. The underfill structure 50 is, and remains, essentially free of contaminants including air and other gases, water vapor and liquid moisture. It should be re-emphasized that the low initial viscosity of liquid resin 60 facilitates complete filling of the volume or space between each semiconductor die 20 and carrier substrate 10, encircling each external conductive element 30 and extending into any crevices 36.

Please amend paragraph number [0085] as follows:

[0085] The third liquid layer 94C is then selectively scanned by a laser beam 112, producing an at least semisolid layer 90C (FIG. 16) above second layer 90B and over the backside 18 of each semiconductor die 20, contiguous with the prior formed layers 90A, 90B. See FIG. 16.

Please amend paragraph number [0086] as follows:

[0086] The next step is illustrated in FIG. 17. Once the structure 48 is completed, platform 120 is elevated above surface level 62 (FIGS. 7 & 8) of liquid resin 60, and the platform 120 with the semiconductor device assembly 40 attached thereto may be removed from apparatus 100. Excess, uncured liquid resin 60 on the surface of the semiconductor device assembly 40 may be manually drained, followed by solvent cleaning and removal from laser beam 110, usually by cutting it free of substrate supports 116, if used.

Please amend paragraph number [0090] as follows:

[0090] If a recoater blade 118 (FIG. 8) is employed, for example, as in forming protective encapsulation envelope 48 on the backside 18 of semiconductor dice 20 in a single layer, the process sequence is somewhat different. In this instance, the support surface 122 of platform 120, with attached semiconductor device assemblies 40, is lowered into liquid resin 60 below surface level 62, then raised thereabove until the backsides 18 of semiconductor dice 20 are precisely one layer's thickness below recoater blade 118. Blade 118 then sweeps horizontally over backsides 18, or (to save time) at least over a portion(s) thereof on which the protective envelope structure 48 is to be built. The recoater blade 118 removes excess liquid material 60 and leaves a film thereof of the precise desired depth 92 above backsides 18. Platform 120 is then lowered so that the surface of the film and liquid surface level 62 are coplanar and the surface of the liquid resin 60 is undisturbed. Laser 108 is then initiated to scan with laser beam 112 and define a first layer 90A ~~which, in this case~~ 90A, which in this case, provides both dam structure 56 and encapsulation envelope 48. A more detailed discussion of this sequence

and apparatus for performing same is disclosed in U.S. ~~Patent~~ Patent No. 5,174,931, previously incorporated herein by reference.

Please amend paragraph number [0095] as follows:

[0095] In practicing the present invention, a commercially available stereolithography apparatus operating generally in the manner as that described above with respect to apparatus 100 of FIG. 8 is preferably employed, but with further additions and modifications as hereinafter described for practicing the method of the present invention. For example and not by way of limitation, the SLA-250/50HR, SLA-5000 and SLA-7000 stereolithography systems, each offered by 3D Systems, Inc. of Valencia, ~~California~~ California, are suitable for modification.

Please amend paragraph number [0099] as follows:

[0099] Alternatively, a self-contained machine vision system available from a commercial vendor of such equipment may be employed. For example, and without limitation, such systems are available from Cognex Corporation of Natick, Massachusetts. For example, the apparatus of the Cognex BGA Inspection PackageTM or the SMD Placement Guidance PackageTM may be adapted to the present invention, although it is believed that the MVS-8000TM product family and the Checkpoint^R ~~Checkpoint~~[®] product line, the latter employed in combination with Cognex PatMaxTM software, may be especially suitable for use in the present invention.

Please amend paragraph number [0100] as follows:

[0100] It is noted that a variety of machine vision systems are in existence, examples of which and their various structures and uses are described, without limitation, in U.S. ~~Patents~~ Patent Nos. 4,526,646; 4,543,659; 4,736,437; 4,899,921; 5,059,559; 5,113,565; 5,145,099; 5,238,174; 5,463,227; 5,288,698; 5,471,310; 5,506,684; 5,516,023; 5,516,026; and 5,644,245. The disclosure of each of the immediately foregoing patents is hereby incorporated by this reference.

Please amend paragraph number [0101] as follows:

[0101] In order to facilitate practice of the present invention with apparatus 100, a data file representative of the size, configuration, thickness and surface topography of the surfaces of for example, a particular type and design of semiconductor device assembly 40 having flip-chip semiconductor dice 20 attached thereto to be underfilled and/or more completely packaged, is placed in the memory of computer 102. If underfill/packaging material in the form of the aforementioned liquid photopolymer resin 60 is to be applied only to one or more (but not all) semiconductor dice 20 of one or more semiconductor device assemblies 40 mounted on support surface 122 of platform 120, camera 124 is then activated to locate the position and orientation of each semiconductor die 20 of each semiconductor device assembly 40 to be underfilled and/or packaged by scanning the semiconductor dice 20 and comparing the features of the semiconductor dice 20 with those in the data file residing in memory, the locational and orientational data for each semiconductor die ~~20~~, including data relating to the die or package dimensions also being stored in memory. It should be noted that the data file representing the design size, shape and backside topography for the semiconductor dice 20 and of traces on carrier substrate face 12 may be used at this juncture to detect physically defective or damaged dice and damaged or defective traces extending out from under semiconductor dice 20 prior to STL underfilling and packaging and to automatically delete such semiconductor device assemblies 40 from downline processing. It should also be noted that data files for more than one type (size, thickness, configuration, surface topography) of semiconductor dice 20 may be placed in computer memory 106 and computer 102 programmed to recognize not only device locations and orientations, but which type of device is at each location so that resin 60 may be cured by laser beam 112 in the correct pattern and to the height required to define the structure 56 and/or envelope 48 being fabricated. In other words, since the backsides 18 of some semiconductor dice 20 may be higher than those of others, once the lower semiconductor dice 20 have been dammed (or encapsulated, as the case may be), the layering process of the invention is then directed only to the semiconductor dice 20 requiring a higher dam structure 56 or encapsulating envelope 48.

Please amend paragraph number [0102] as follows:

[0102] The liquid photopolymer resin 60 selected for use in this invention may be any polymer which exhibits appropriate polymerization properties, has a desirable dielectric constant, is of sufficient (semiconductor grade) purity, has a relatively low viscosity, has sufficient strength to withstand mishandling, and which that is of sufficiently similar coefficient of thermal expansion (CTE) to that of semiconductor die 20 so that the polymer structure (i.e., package) and the semiconductor die 20 itself are not stressed during thermal cycling in testing and subsequent normal operation. In addition, depending upon the thickness of resin layers desired to be formed, the liquid photopolymer resin 60 may have a surface tension which that prevents it from flowing out of a device-to-substrate spacing in the range of about 1 to about 28 mils.

Please amend paragraph number [0106] as follows:

[0106] Further, the high precision of the STL process results in semiconductor device assemblies-~~40~~ 40, which are of enhanced uniformity in package coverage and dimensions. Surprisingly, the package dimensional tolerances achievable through use of the present invention are more precise, e.g., three times more precise than those achievable in a transfer molding system. Moreover, the process is very rapid, resulting in enhanced underfilled and packaged semiconductor device assemblies 40 at a significantly lower cost. Post-cure of semiconductor device assemblies 40 formed according to the present invention may be fully effected and accelerated in an oven at a relatively low temperature such as, for example, 160 degrees C.